WHAT IS CLAIMED IS:

1. A method of forming metal wiring in a semiconductor device comprising:

forming a bottom metal pattern on a semiconductor substrate;

forming an insulating layer on the semiconductor substrate including the bottom metal pattern;

forming a first photoresist pattern for forming via hole on the insulating layer;

forming an unfinished via hole by removing the insulating layer selectively for a prescribed thickness using the first photoresist pattern as a mask;

removing the first photoresist pattern;

forming a second photoresist pattern for forming damascene pattern on the insulating layer around the unfinished via hole;

forming a damascene pattern by removing the insulating layer selectively using the second photoresist pattern as a mask;

removing the second photoresist pattern; and

forming a metal wiring via damascene contact by filling metal in the damascene pattern.

2. The method of claim 1, wherein a low temperature oxide is used for the insulating layer.

3. The method of claim 2, wherein the oxide is formed at the temperature of 150~500℃.

4. The method of claim 1, wherein the unfinished via hole is formed to make the thickness of the insulating layer remaining inside the via hole equal to or less than the thickness of the upper part of damascene contact.

5. The method of claim 1, wherein the damascene contact is made of Cu, Al, W, Pt, Co, Ni, or alloy thereof.

6. The method of claim 1, wherein the damascene contact is formed by depositing metal on the insulating layer including the damascene pattern and planarizing the metal by CMP process.

7. The method of claim 6, wherein the metal is deposited by electro-chemical deposition or dry deposition.

8. The method of claim 1, wherein the insulating layer is formed to have a thickness of 1,000~20,000 Å.